Cornell University Autonomous Underwater Vehicle Project Team Technical Documentation: Orion and Sirius AUVs 2024-2025

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***Abstract*— Orion and Sirius are the two autonomous underwater vehicles that represent Cornell University in the AUVSI RoboSub 2025 competition. Orion is our newest vehicle, developed for the 2024-2025 cycle with the main focus on reliability. While Sirius remains a fully capable submarine, Orion introduces refinement-focused updates based on learnings from Sirius. Together, these two vehicles allow us to prepare thoroughly for competition and complete as many tasks as possible with confidence.**

I. Competition Strategy

This year CUAUV's competition strategy emphasizes reliability as well as flexibility across both vehicles. Based on lessons from past years, we adopted a lower-risk design approach to maximize testing time and focus engineering efforts where they matter most. Mostly maintaining the square-shaped frame and UHPV design from Sirius, a few modifications were made to support a novel manipulator design and new, larger battery pods. This design cycle prioritized reducing risk in structural components early on, with increased testing time being the main motivator. New battery pods were created to accommodate our custom Battery Management System, and a reworked hydrophone system uses a new approach in terms of architecture for improved acoustic performance. The team collectively agreed that perfecting a working design was the best way to prepare for competition as well as ensure the transfer of knowledge to younger members. Both Orion and Sirius are prepared to perform a wide range of tasks, ensuring that any issues during competition can be mitigated by redundancy.

CUAUV's large and experienced team allows us to pursue this parallel development model while still involving all members in impactful technical work. The team takes pride in being able to teach new members through mission critical projects, showcasing the trust and support built within the team. Vehicle testing mainly focused on areas such as actuation and vision perception, with the intent to build on the experiences of last year through iteration. This balance of innovation and redundancy was achieved with the competition strategy of attempting as many tasks as possible.

II. Design Strategy

A. Mechanical Systems

Our newest AUV, Orion, seeks to iterate on the many novel design changes incorporated into our previous AUV, Sirius. Similarly to Sirius, Orion has a reduced number of separate enclosures, opting to condense core subsystems, such as our GX sensor and killswitch, to our Upper Hull Pressure Vessel (UHPV). However, we continue to isolate our more complicated systems, such as our hydrophones system and manipulator, which allows these to be modular, easy to prototype, and backward compatible with previous AUVs. Through our extensive testing with Sirius, as well as Finite-Element Analysis (FEA) simulations, we

have further optimized Orion's design by reducing the overall volume and weight of its core subsystems. Incremental changes to our frame, PCB mounting racks, and UHPV have allowed us to shave off a few additional pounds, keeping us under the weight penalty with all sub-systems installed.

Fig 1. Orion Upper Hull Pressure Vessel.

1) UHPV: Orion sports another rectangular or "lunchbox-style" UHPV, with some small design changes to make a more reliable seal. Last year, during the initial testing, Sirius suffered from many small leaks at its welded joints, so Orion's UHPV was designed for subtractive manufacturing to avoid this issue. The main bore seal engaged when opening and closing the lid has also been modified to support a thicker o-ring, and the clearance gap was machined to a tighter tolerance to make the lid easier to remove without compromising sealing strength [1].

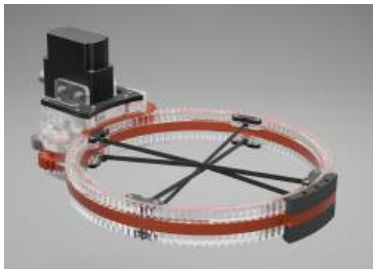

Fig 2. New Manipulator Design.

2) Manipulator: This year, we took a different approach when designing our manipulator, opting for a more flexible design that can pick up a wide range of objects. This allowed us to begin prototyping and iterating on our geared hoop far before the release of the rulebook specifying the size and shape of the competition objects. A careful selection of materials, including ABS, TPU, and aluminum, allows the manipulator to be lightweight, compliant, and strong. A series of gears connected to a servo rotate the two larger hoops against each other, ensnaring game elements in its web. An adjustable passive friction plate also ensures that the hoops are properly engaged with the gear system, and can be easily tuned up between competition runs.

Fig 3. Battery Pods.

3) Additional Improvements: Some of our other subsystems have also seen some small changes. Our battery pods have been redesigned to more easily accommodate both our batteries and Battery Management Boards, which should make them safer and easier to access when needed. Orion's down camera enclosure has been designed with thicker o-rings, making it less prone to leaks as a result of installation errors or standard wear-and-tear. Hydrophones and transmit enclosures on both AUVs have also been updated to best suit the latest version of their respective printed circuit boards and electrical integration.

Fig 4. Full Render of Orion.

B. Electrical Systems

As in previous years, both of our current AUVs' electrical systems emphasize customization and redundancy. They both feature modular layouts,

enabling "hot-swapping" of custom PCBs and allowing CUAUV to rapidly integrate new features without a full redesign. This allows the electrical system to be modified according to the challenges of the competition. In this vein, Orion's electrical system seeks to improve upon several of our existing projects/features, including our acoustics systems, sensors, and power management.

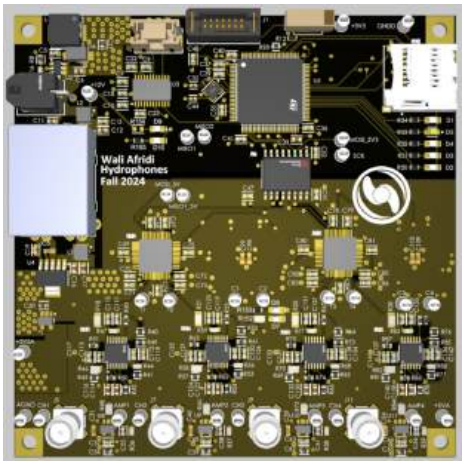

Fig 5. New Hydrophones Board.

1) Acoustic System: CUAUV underwent a revitalization of our acoustics system to increase reliability and eliminate bottlenecks which had caused numerous issues in the past [3]. Our new hydrophones board interfaces with 4 transducers, digitizing analog signals and applying dynamic gain control, Gaussian FIR filtering, and phase analysis to extract heading and elevation angles at the various required pinger frequencies. All of the signal processing has been moved to an embedded solution via an STM32 microcontroller, freeing up compute space on our main Jetson computer, and removing the need to send hundreds of thousands of samples per second between enclosures.

We also worked to optimize the efficiency of our custom communications pinger. Piezoelectric resonators typically have a very high Q-factor, meaning that driving not on the resonant frequency leads to a significant decrease in the mechanical output power. Previously, we have used frequency-shift keying (FSK) to encode binary messages through the water. This resulted in limited efficiency, which was a key point of improvement this year. CUAUV now uses On-Off keying (OOK) to encode our inter-vehicular communications messages. Not only does this increase efficiency and allow communication at further distances, this simpler protocol makes messages fast and easy to decode on the receiving side.

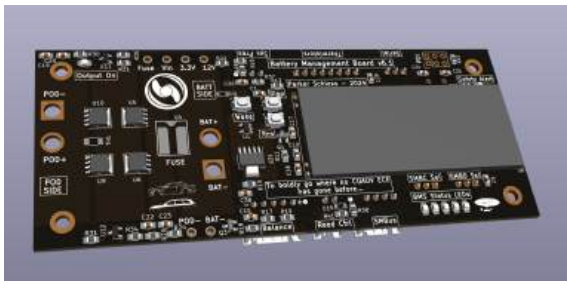

Fig 6. BMB Board.

2) Power Management: CUAUV took another step forward with the reliability and capabilities of our power flow architecture. Building upon what we began last year, our battery management boards continue to provide cell voltage balancing, battery health monitoring, reverse polarity protection, and more. The board also makes this information accessible in and out of the sub, with UART communication and an on-board OLED screen. Our new and improved Merge board ensures load balancing between the two external battery pods, and is rated for up to 60 Amps of continuous current draw.

3) Additional Improvements: This year, we also made a number of smaller improvements. These included upgrading our depth/pressure sensor to the Blue Robotics Bar02 for increased precision and accuracy, as well as the addition of fans within the Upper Hull Pressure Vessel to increase airflow to high-power boards. Additionally, we further iterated on the serial communication board, which had undergone a more major redesign last year, to reduce size and minimize signal crossing.

C. Software Systems

This year we emphasized reliability, flexibility, and performance. In addition to following this principle in our mission designs, we worked on major redesign and refactoring of our critical infrastructure including the vision system, the mission system, etc. We worked on integration of key components such as a new Waterlinked DVL to Orion. By equipping both subs with similar capabilities, we hope to build redundancies. In the

case that one vehicle encounters hardware issues, the other is capable of stepping up.

1) Vision Pipeline Redesign: In previous years, our vision system suffered from occasional crashes due to implementation flaws. Implemented as a triple buffer, it used traditional reader-writer locks to manage buffer access by the camera capture sources (writer) and vision modules (reader). If a writer process crashed while holding a lock, the buffer could become deadlocked, requiring manual intervention to free up resources. These failures disrupted testing and raised concerns about reliability during competition.

To address this, we created a camera messaging framework. While still a triple buffer design, it changed drastically in its concurrency and synchronization mechanisms. We discarded the reader-writer locks in favor of lock-free seqlocks: each buffer slot tracks version numbers before and after writes using atomic counters. Writers can update buffers without blocking, and readers detect whether a write occurred mid-read by comparing version counters. If the versions do not match, the read is retried. This ensures consistency without requiring any process to wait, avoiding deadlocks and preventing starvation. In addition, updates include support for data types like uint8, float32, and float64, providing capability for both RGB imagery and high-precision depth streams.

Alongside the camera messaging framework, we also created a new capture source system that standardizes how camera processes interact with the pipeline. Each camera process is built from a shared base that handles threading, timing, and memory writes. Camera-specific logic is defined through user-defined logic (UDL) functions that run in parallel and send images to different directions. For example, the ZED camera can stream forward, downward, and depth images at the same time, so different vision modules can access the data they need without duplication. The system also allows us to limit the frame rate for each stream, giving us more control over how processing resources are distributed.

Together, these changes make the vision pipeline more stable, scalable, and provide a simplified development platform.

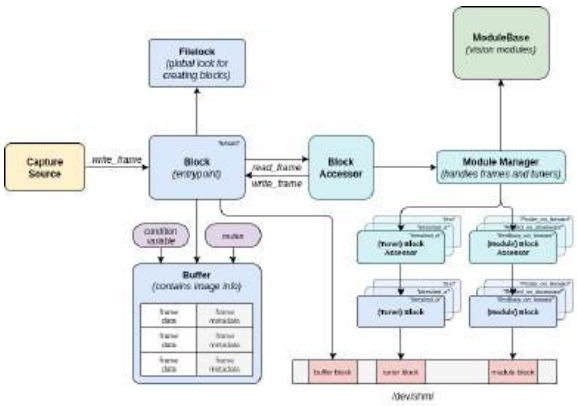

Fig 7. New vision buffer system architecture.

2) YOLO Pipeline Improvements: YOLO still remains as one of the best performing object detection models out there, and we still are using it in this upcoming competition. This past year, we have made improvements to our developer operations that have significantly improved the rate at which we have been able to train, evaluate, and deploy new model versions.

We refined our YOLO pipeline to support faster training and simpler development of detection modules. Instead of training YOLO models on the cloud, we now train YOLO models locally using a Python script integrated with Roboflow. This gives us faster iteration time, full control over training parameters, and removes friction in our operations.

We tested different flavors of YOLO detection, including pose to identify key points within mission element structure, segmentation to provide more precise contour outlines instead of bounding boxes, and oriented bounding boxes to provide rotational information. We found that pose and segmentation did not generalize very well to new footage and decided to stick with YOLO-OBB as our primary model.

The YOLO model is integrated into our vision pipeline as a single vision module that is continuously running. After the core model makes an inference call on a video frame, optional custom-written post-processing logic is applied to each individual object detected in a structure we call object “handlers”. To save on compute, we can optionally choose to turn off and on specific object handlers through shared memory to save on compute power. This approach provides both the powerful results of machine learning computer

vision and custom control over the information we decide to accept.

Each pool test each week, we collected footage that captured a wide range of lighting conditions, angles, and distances of the mission elements. After annotating and training a new YOLO model, we tested its performance, identifying any cases where performance was poor and aimed to re-capture more footage in these areas.

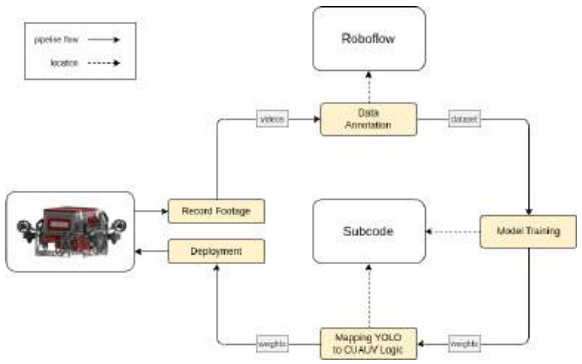

Fig 8. Diagram of our YOLO data collection pipeline.

3) WaterLinked DVL A50 Integration: In Spring 2025, we integrated the WaterLinked DVL A50 on one of our submarines, giving both vehicles onboard DVL capability for the first time. Having DVLs on both submarines is a major upgrade as it allows us to use accurate positional controls on both Submarines.

III. Testing Strategy

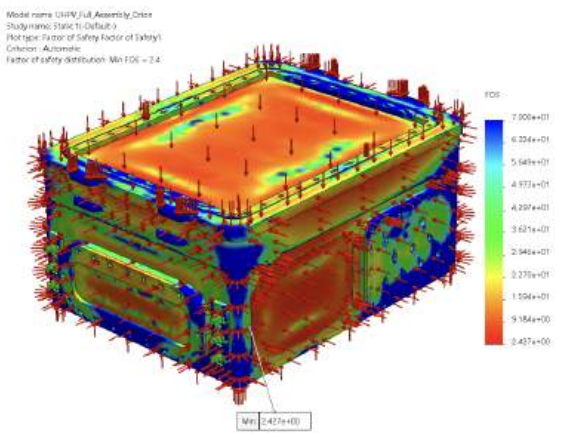

Fig 9. Factor of Saftey Simulation.

A. Mechanical

During the design portion of our production cycle, we test all of our physical systems using Solidworks' Finite Element Analysis (FEA) simulations. For our sealed enclosures, we run a pressure simulation which models how our designs will handle forces experienced at 30 feet of depth, focusing on their maximum displacement and factor of safety against yield strength. For our actuators (including our manipulator and torpedoes/droppers launcher), we model the forces produced by our servos and springs. These simulations not only help us to determine if our final designs should last the competition environment, but also let us make informed decisions on how to reduce weight or choose proper materials/thicknesses in our designs.

Once machined and mechanically integrated, all of our sealed enclosures are subject to a thorough leak-testing process. Enclosures are lined with shop towels, particularly around sealing surfaces, and are sunk to the bottom of our pool (12 feet) for 8 hours overnight. Once recovered, the exterior of our enclosures are dried off, the enclosures are carefully opened, and any signs of water are searched for. If the interior is completely dry, the enclosure has passed and can be electrically integrated. If any dampness is detected, then we use the shop towels to determine the most likely cause of the leak, and re-evaluate the failing seal (using our new o-ring sealing guide as a reference).

New this year to our leak testing is a pressurized chamber that can be used to initially screen for any sealing issues in our smaller enclosures. For a test, the pressure chamber is filled with water, the internal pressure is set to simulate a 15 foot water depth, and the pressure is regulated indefinitely for as long as we want to test the enclosure for (usually overnight). Since the pressure chamber is still new, we have not used it in lieu of an overnight pool leak test. However, once we are more confident that it provides an accurate analog to our traditional pool test, we plan on using it to greatly reduce the number of overnight pool tests we schedule, accelerating our overall testing and integration timeline.

B. Electrical

This year our senior electrical subteam members, each of whom worked on one of the historically more challenging PCBs, underwent a two-stage design process in order to improve reliability and maximize opportunities for testing and design iteration. Of particular interest were PCBs featuring heavy redesigns, such as those on the power path. Both the battery management board and the merge board, which is responsible for load balancing, underwent load testing, with the parameter for success being 60A for 10s and 30A continuously without overheating (based on current measurements from past AUVs). These boards did not initially meet the parameters for success and were majorly improved in the second design and testing stage.

Additionally, bench testing for all boards that communicate with the Jetson computer is made easy via the Serial Debugger. This is a piece of software written by CUAUV that communicates directly with the ATXMEGA MCU present on all of the "smart" PCBs. The program is able to read and write serial variables over RS232, providing accessible low-level control to our electrical team. Finally, the aforementioned modular electrical design philosophy enables easy, reliable PCB testing. Throughout the year, the software team tests code in the pool using last year's AUV, Sirius. Many of the new PCBs were compatible with this design and could be swapped in. This enabled the team to validate many of our designs in real-life conditions before the completion of our new competition AUV, with the thruster, actuator, infrastructure, and merge boards all tested before the end of the school year.

C. Software

We develop our mission logic iteratively in the following steps. We first test our missions in a 3D simulator that we developed many years ago. We use this to verify the correctness of the core components. Although our 3D simulator does have a vision component, it is often too idealized, so we also test our vision code on recorded pool footage using a video playback application that we have developed.

When the fundamental logic is in place, we further test our missions in the pool to fine-tune our vision algorithms [4] and consider any edge cases the simulations may not have accounted for. Testing our competition strategy is done bottom-up. We begin by running each individual task, from the gate, torpedoes, etc. on their own, assuming that the mission elements are in sight and verifying the submarine completes each task successfully given this precondition. When all tasks have been thoroughly tested, we chain the tasks together in one "master" mission, handling edge cases and searching logic. While actively running our missions, we simultaneously record the camera footage in the background, which provides training data for our YOLO models, and also provides testing footage that can be run on our playback application when iterating on our vision modules.

We repeat this process until our mission consistently achieves its mission objectives in the water.

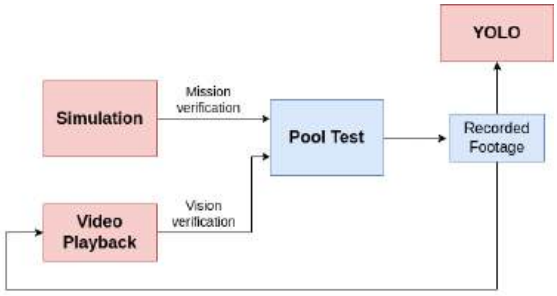

Fig 10. Software testing loop.

IV. Acknowledgements

CUAUV would like to thank all the individuals and organizations who have supported us over the past year, including Cornell's MAE, ECE, and CS departments. Thank you to the Fischell family for their ongoing support and for sparking a lifelong interest in AUVs in our team members. CUAUV would like to thank our adviser: Professor Hunter Adams. Special thanks to the Director of Cornell Aquatics, Brigitta Putnam; the MAE Director of Instructional Laboratories, Matt Ulinski; we would like to give special thanks to Lauren Stulgis, Kate Reiter, and Gibran el-Sulayman. We would also like to thank all of our corporate sponsors, without whom we would not be able to compete.

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[1] Parker O-Ring Handbook, ORD 5700. Parker Hannifin Corporation, Lexington, KY, USA, 2021
[2] G. Bradski and A. Kaehler, OpenCV. Dr. Dobb's journal of software tools, vol. 3, no. 2, 2000.
[3] B. Benson, "Design of a Low-cost Underwater Acoustic Modem for Short-Range Sensor Networks," 2010.
[4] G. Bradski and A. Kaehler, OpenCV. Dr. Dobb's journal of software tools, vol. 3, no. 2, 2000.

APPENDIX A

Component	Vendor	Model/Type	Specs	Source	Cost	Year
Sirius Frame	Datron	Custom Aluminum Waterjet	Custom	Custom	Sponsored	2024
Orion Frame	Datron + Kontrast 3D	Custom Aluminum Waterjet	Custom	Custom	Sponsored	2025
Outsourced Machining	Xometry	Custom Aluminum CNC	Custom	Custom	$3,100	2025
Aluminum Stock	Midwest Steel	Various	Various	Purchased	$800	2025
Aluminum Anodization	Surface Finish Technologies	N/A	N/A	Purchased	$1,100	2025
Acrylic Tubing	Polymer Plastics	N/A	Custom	Custom	Sponsored	2025
Waterproof Connectors	SEACON HUMMER/ WET-CON	Dry/Wet connectors	Custom	Custom	$1,675	2018
Thrusters + Propellers	Blue Robotics	T200	Brushless Thruster	Purchased	$2,312	2018
Motor Control	Blue Robotics	Basic ESC	Speed Control	Purchased	$400	2018
Actuators	Blue Trail	SER-2020	230º Underwater Servo	Purchased	$495	2024
Battery	HobbyKing	Multistar 4S	High Capacity, LiPo Battery	Purchased	$400	2024
DC Voltage Regulator	Cincon	CHB75-12S12	Voltage Regulation	Purchased	$76.28	2024
CPU/GPU	NVIDIA	Jetson Orin Nano	Six 2GHz, Arm8Cores	Purchased	$500	2025
Compass and IMU	LORD Microstrain	3DM-GX3 / 3DM-GX5	AHRS	Purchased	Sponsored	2018

Component	Vendor	Model/Type	Specs	Source	Cost	Year
Doppler Velocity Log (DVL)	WaterLinked	A50	DVL	Purchased	Sponsored	2024
Cameras	IDS	UI-6230SE UI-5140CP,	Cameras	Purchased	Sponsored	2018
Camera	FLIR	BFS-PGE-16S2C-CS Blackfly S GigE	Cameras	Purchased	$175	2024
ZED Camera	StereoLabs	Zed 2i	Cameras	Purchased	$499.99	2024
Hydrophones Processor	NXP	FRDM-K64F	Hydrophones	Purchased	$52.35	2024
Hydrophones, Teledyne Marine	RESON	Acoustic transducers	Hydrophones	Purchased	N/A	2018
High Level Control	CUAUV	6-DOF Dual Quaternion and YPR	Linear Least Square PID	Custom	N/A	2015
Vision Algorithm	OpenCV	OpenCV4	Transparent GPU Support	Purchased	Free	2024
Vision Algorithm	YOLO	YOLOv8	Transparent GPU Support	Purchased	Free	2024
Depth Sensing	ZED	ZED SDK 4.2	N/A	Purchased	Free	2025
Acoustics	CUAUV	Custom DSP	N/A	Custom	Free	2024
Localization and Mapping	Mur-Artal	ORB-SLAM2	Modified	Purchased	Free	2024
Autonomy	CUAUV	Mission Planning system	N/A	Custom	Free	2024
Software	CUAUV/FSF	GNU	N/A	Custom	Free	2024

APPENDIX B: ELECTRICAL

SERIAL BOARD

The serial board acts as a communication interface between many of the submarine's electrical subsystems (primarily the electrical boards) and the main computer in the submarine (the Jetson). It utilizes receive (RX) and transmit (TX) signal lines from connected subsystems, managing voltage level transitions between RS232 and TTL specifications, and converting serial (UART) data lines to USB. Connected to the main computer through a single USB-C connector, the board efficiently handles up to 16 RX/TX pairs,facilitating comprehensive data conversion and transmission within the submarine's electrical infrastructure.High Level Description The serial board utilizes a low-dropout regulator to convert isolated +5V from the connector to +3.3V, which powers all of the components on the board. In addition, a second LDO is used to generate a stable +1.1V for the USB Hub IC. Serial board receives an isolated power source to protect its sensitive components from noise and ESD. In addition, there is a supply voltage regulator that turns on the serial data chips only when a reliable voltage threshold is met.

The remainder of the board is dedicated to serial data. USB data coming in from the type-C connector is split into 4 ports by a USB hub IC. Each of these USB ports corresponds to an identical set of USB to UART ICs (FTDI circuitry). Each of these circuits converts a USB signal to up to 4 RX/TX pairs (ports) and vice versa. The USB-UART circuitry utilizes an EEPROM for configuration and a shift register for LED display of channel activity. Yellow LEDs correspond to TX line activity and Blue LEDs correspon to RX line activity. Serial port transceivers then shift the UART signal levels from TTL to RS-232 before they travel through the backplane to reduce the noise they experience.

Implementation

The TUSB4041I device provides support for USB battery charging; however, this feature is disabled on each of the ports by pulling the corresponding pin to GND. The TUSB4041I device can also be configured for power-switched applications using either per-port or ganged power-enable controls and over-current status inputs; however this feature is also disabled by pulling over-current pins to GND. The ports are set to per-port controls by pulling the Ganged pin to GND as well. A 24 MHz ±30ppm 20pF 30 Ohms Crystal is used to drive an internal oscillator with the proper specifications. Both the external interface and EEPROM are disabled by pulling the corresponding pins to GND. An LDO is utilized to generate a stable +1.1V from the provided +3.3V.

USB-UART Circuitry

The FTDI chips responsible for the USB-UART conversion are a crucial feature of the serial electrical system. Each chip handles 4 RX-TX pairs (4 RX signals and 4 TX signals) and converts the serial (UART) data to a single USB differential signal pair. This USB signal is accompanied by a transient suppressor to stabilize the sensitive signal and provide ESD protection. Internally, the FTDI chips contain an LDO to generate +1.8V, but additional decoupling capacitors are added along the VREG and VCORE pins for integration. The FTDI chips also require 12MHz crystals, different from team common. Each FTDI interfaces with an EEPROM to configure its vendor and product ID number in order for the main computer (Jetson) to recognize each FTDI as unique entities. Additionally, the EEPROM allows for the main computer to configure where data packets go to and come from by 'naming' respective ports downstream. Finally, the shift register associated with each FTDI utilizes the USB data to recognize when a signal transmission occurs on any of the 8 TX/RX lines, illuminating the corresponding LED. This visual feedback mechanism provides insights into the submarine's communication status, offering valuable assistance in the debugging process.

Serial Port Transceivers

Also known as the level shifters, the ADM3307 and the ADM3310 raise outgoing transmit signals to RS-232 (up to -15V/+15V) and lower incoming receive signals to TTL (+3.3V). This conversion is crucial as signals to and from the USB-UART ICs must operate at TTL levels, while higher RS232 voltages play a critical role in minimizing noise on longer-distance signals throughout the electrical system. These two components differ only in their channel configurations, with the ADM3307 featuring 5 RX channels and 3 TX channels, and the ADM3310 having 5 TX and 3 RX channels. Utilizing two of each ensures the desired 16 TX and 16 RX lines. For schematic purposes a consistent naming convention is employed, where uppercase nets signify higher RS232 voltage, and lowercase nets represent lower TTL voltage.

Connector

The connector supplies 5V power to the serial board and sends/receives RX/TX lines from other boards via the corresponding connector pins on the backplane.

Low-Dropout Regulator

The TPS7A4533 low-dropout regulator (LDO) reduces the incoming +5V to +3.3V, supplying power to all circuitry on the serial board. Use of a TPS3809K33 voltage regulator, ensures a stable supply to sensitive components by monitoring the voltage against ground. During startup, ICs are not initialized until a lower threshold of +2.93V is met. In case of a voltage drop below the acceptable threshold, a reset signal is transmitted to the USB hub and each USB-UART IC. The reset signal, activated by pulling it to ground, is controlled by a physical reset switch on the board, allowing manual initiation when pressed.

Layout

Considerate thought is put into the layout of serial board before beginning in order to ensure sensitive signal traces do not experience cross-talk or EMI that undermine the signal integrity. The serial board has four copper layers, with the inner two being dedicated to a +3.3V power plane and a solid GND plane. The FTDIs, USB differential pairs, and USB Hub are placed on the back of the board so that there is a solid GND plane beneath these elements to reference. Differential signal pairs are the most sensitive to interference and care is taken to make sure that both traces are of equal length and that the pitch does not ever become too large. Additionally, no components or large traces are placed across these signals on either side of the board. Great effort is made to reduce the amount of signal traces that cross one another, but when they do they do so perpendicularly to reduce interference as much as possible. Previous iterations of this board had become incredibly optimized with positioning to reduce signal crosses and trace length; however, the new requirement for a USB hub significantly decreased available space and introduced more sensitive USB data lines. LEDs to indicate signal traffic are placed in a line at the top of the board and are labeled for quick debugging purposes. As was previously done in KiCad, a layout-replication tool in Altium was used to copy and paste the FTDI circuitry for each FTDI sheet.

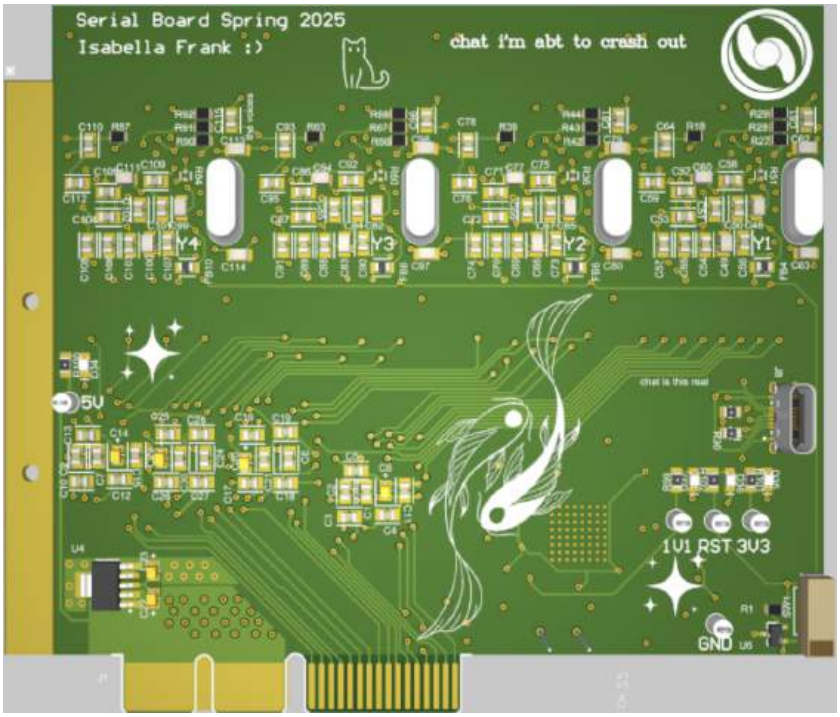
This iteration of the serial board is smaller than last year's so it was crucial to make sure that space was used efficiently. The order of the signals from the backplane connector to the level shifters, and from the level shifters to the FTDI circuitry was rearranged to reduce the need for signals to cross over one another. This change in ordering of the TX/RX pairs resulted in this iteration of the board not being backwards compatible with Orion. The FTDI circuitry was also made more horizonatally compact - the extra vertical space necessary was accounted for by the removal of the mini-USB ports that were kept on the previous iteration of the board.

The first iteration of the layout had the USB-C port facing upwards, which made it very difficult to fit a cable into the connector while also populating the circuitry surrounding FTDI 1. The second iteration has a USBC port that faces straight up perpendicular to the surface of the board to prevent this.

Software Walk-Through

Four FTDI configuration files (one per chip) attribute various flags to each IC, but are otherwise identical. The strings corresponding to the FTDI's manufacturer, product number, and serial reference are all renamed for easier detection purposes when attempting to identify the otherwise identical FTDI chips. In addition to defining various flags, these files also declare the FTDI chips as self-powered.

Software must be made aware of the FTDI chips' individual configuration information – this includes the serial reference of each FTDI, as well as which signal pairs correspond to which ports on the FTDI chip.



Serial Board.

HYDROPHONES

Abstract

The hydrophones board is responsible for acoustic data acquisition and signal processing to enable pinger tracking and inter-vehicular communication. The board takes input from 4 TELEDYNE RESON TC4013 piezoelectric transducers, and outputs critical data regarding pinger direction and recieved data via serial communication to the main submarine computer.

Design Requirements

- Size: 3.75" x 3.75"
- Channels: Up to 4 coaxial inputs (from four separate elements), still capable of using 3 coaxial inputs
- Data bands: Simultaneously 25-40 kHz for pinger tracking (competition specified frequency), and 46-56 kHz for data transmission

- Output data: RS232 UART
- Voltage supply: 12V

Design Updates

This revision of the Hydrophones board attempts to do all of the necessary signal processing on-board using an STM32 microcontroller. The past several revisions of this board utilized an FRDM development board with integrated ethernet to pass all recieved data samples to the Jetson and allow all the signal processing to happen on the Jetson.

High Level Description

First, the incoming sound-pressure signals are amplified using voltage feedback amplifiers because they are low amplitude signals represented by total charge rather than voltage. Then, the signals are passed through bandpass filters to avoid aliasing and low-frequency rumble. Each channel has two separate bandpass filters, one with a passband corresponding to the communications frequency range, and the other with a passband corresponding to the pinger frequency specifications. After these filters, the two sets of signals, pinger and comms, are digitized using simultaneously sampling Analog-to-Digital Converters (ADCs) with programmable gain input stages; the gain loop for the ADCs is run on the MCU. Then, the samples are processed on the STM32 MCU and information such as the heading toward the pinger and communicated messages are sent to the Jetson via RS232 serial out of the enclosure.

Implementation

Hydrophone Elements: The Teledyne TC4013 is used for all four elements. Because phase difference is used for determining ping location, the elements must be positioned less than half of one wavelength away from each other (1.50 cm at 40 kHz) to prevent spatial aliasing. This type of transducer can be quite expensive, so cost was a deciding factor in selecting the TC4013.

Bandpass Filters: There is a lot of low frequency noise in the environment, so a bandpass filter is used to prevent the ADC from dropping the gain and lowering the dynamic range of the signal of interest. The separation of communications frequencies and pinger frequencies is essential before sampling because one could potentially overpower the other. The competition pinger frequencies will range from 25 to 40 kHz in 0.5 kHz increments. The transmit board communication frequencies will range from 46 to 56 kHz.

After the filters were designed by the ”Filter Wizard” application, they were verified in LTspice simulation to ensure they exhibited the desired frequency response. It is worth noting that due to the very low passband ripple implemented here, these 8th order Chebychev filters are very close to being 8th order Butterworth filters, especially when glancing at the plots. If the passband ripple were any lower perhaps it would be appropriate to call these Butterworth filters instead. Additionally, because resistor values are slightly inaccurate and some resistor values are difficult to find, it is unexpected to perfectly recreate these filters after population.

Analog-to-Digital Converters: This board uses four AD7264 chips, selected for their two 14-bit simultaneous sampling ADCs with SPI capabilities. A goal of 200 kHz sampling rate is the hope, which is well above the Nyquist sampling rate. Another important feature is that the chip includes a programmable gain amplifier with good resolution between 1x and 128x. The operating range varies from 1 to 100 meters, which results in vastly different signal strengths, making this feature extremely important. An external reference is used instead of a built in reference so that all chips can use the same (mid-rail) reference. The SPI bus is designed so all four signals in each set are sampled simultaneously in order to avoid unwanted phase differences. All chips use a clock generated by an SPI port on the microcontroller, the controller. Then the peripheral select signals are alternately asserted on the pinger ADCs or the communications ADCs. The data from the two active chips (with two ADCs each) is read by the MCU using a controller and designated peripheral port.

Microcontroller: This is the first revision of the board to use an STM32H750VB microcontroller, on which I will attempt to run digital signal processing algorithms in the firmware on all of the recieved input data and output the most critical information through writable SHM variables.

Power Rails: The board recieves an isolated 12V power and ground from the DCDC board, which it steps down using a LDO-Replacement buck converter to 3.3V to be used on all of the digital components. An additional isolating DCDC steps the voltage down to 5.5V and feeds this into an LDO that generates a stable 5V for our analog. Because our 5V is in reference to 0V ground, we also generate a 2.5V reference voltage using another LDO that is also used by the analog components. Two digital isolators are used to transfer SPI communication between the analog and digital sections.

Firmware Overview

ADC DMA Input and Gain Scaling + Normalization The board uses the SPI0 and SPI1 channel to pseudo-simultaneously read from all 4 channels of either the pinger tracking filters or the communication filters. We use a 200kHz sampling rate via a 8MHz SPI clock frequency. This data gets sent straight to corresponding circular DMA buffers for each channel.

Because there is a large uncertainty in our distance to the pinger that we are listening to, and the strength of signal goes as the inverse square law, we need to adjust the gain prescaler to get reasonable values out of the ADC at all distances.

We use the programmable gain amplifier (PGA) built into the AD7264 to handle this. After each sampling batch, the firmware calculates the RMS value of the signal and adjusts the gain for the next batch accordingly. Samples are then normalized based on the gain used at the time they were acquired.

Single Frequency DTFT (Sines and Cosines Accumulator): To determine the presence of a ping at a specific frequency, the firmware performs a Discrete-Time Fourier Transform (DTFT) at a single frequency. We compute the in-phase (I) and quadrature (Q) components by maintaining accumulators for sine and cosine products of each input signal. This is equivalent to correlating the input with a sine and cosine at the expected frequency.

This method allows us to efficiently track signal amplitude and phase without requiring a full FFT. We store the I and Q values over a short time window to allow further filtering and magnitude estimation.

Lowpass Filter: To reduce noise and transient artifacts, this magnitude signal is passed through a Gaussian lowpass FIR filter. The filter is designed to retain the shape of the ping envelope while removing high-frequency components that could trigger false positives.

This filtering is critical to suppress the influence of impulsive or transient noise and to improve the accuracy of subsequent trigger and phase calculations.

Triggering: The filtered magnitude signal is continuously monitored. A ping is considered detected when the filtered magnitude exceeds a programmable threshold. To avoid spurious triggers due to multipath interference or reflections, we introduce a refractory period after each trigger. Only samples acquired shortly after the trigger event are used for further phase analysis.

The triggering logic is configurable over UART by changing the detection threshold. Only pings that meet the magnitude and timing criteria are passed on to the next processing stage.

Relative Phase Calculation: Once a ping is detected, the I and Q values of each channel are frozen and used to compute the phase using atan2(Q, I). The phase of one hydrophone is chosen as the reference (typically the front-facing one), and the relative phases of the remaining hydrophones are computed by subtracting the reference phase.

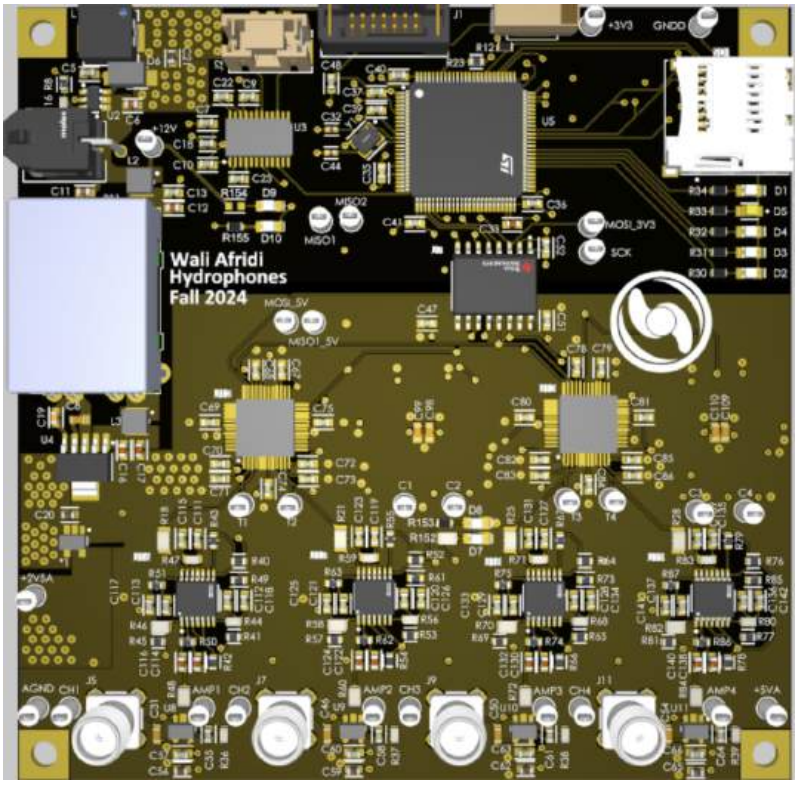
These relative phases are the key input to both heading and elevation estimation. A simple calibration routine can be used to correct for fixed phase offsets caused by hardware tolerances.

Heading and Elevation Angles: Using the relative phase differences across the hydrophones, the system estimates the angle of arrival of the pinger signal. For heading, a straightforward phase difference model is used assuming far-field approximation and linear hydrophone placement.

Elevation angle estimation is more complex and may use either a maximum likelihood estimator or a Bayesian approach based on a model of the signal propagation. In either case, the result is sent along with a confidence score via UART to the Jetson.

AUV Serial Library for STM32: To communicate heading, elevation, and other data to the Jetson, the existing AUV serial protocol stack (uart.c and uart.h) is being adapted to run on the STM32 platform. This includes functions for encoding/decoding variable messages, reading/writing UART registers, and managing protocol state machines.

The firmware maintains a set of writable variables such as TrackFrequencyHz and SDCardRecord, and outputs variables like HeadingAngleDegreesRelative, ElevationAngleDegreesRelative, and TrackConfidence. These variables are exchanged using a simple, fixed-format binary protocol at 115200 baud.



Hydrophones Board.

DCDC

Abstract

The DCDC board must convert the 16V battery power from Merge board and create 3 voltage supplies that the rest of the electrical system can use. These supplies are isolated 12 volts, isolated 5 volts, and an unisolated 7.4 volts. This semester, I modified the DCDC board to add grounding strategies, improve layout, and heat management. I also added LEDs to both sides of the board for better visibility

Design Requirements

The DCDC board must satisfy the following requirements:

- Size: 4.331 x 1.102 x 3.287 inches
- Output supplies: Isolated 12V, Isolated 5V, Unisolated 7.4V, ISOGND
- Voltage supply: Unisolated 16V

Previous Designs

The team made a switch to Altium this semester and we wanted to move all of the boards in the electrical system over to Altium, so I volunteered to move DCDC. the previous design is functional so this board uses the same components, but I have added ferrite beads for better grounding and isolation.

High-Level Description

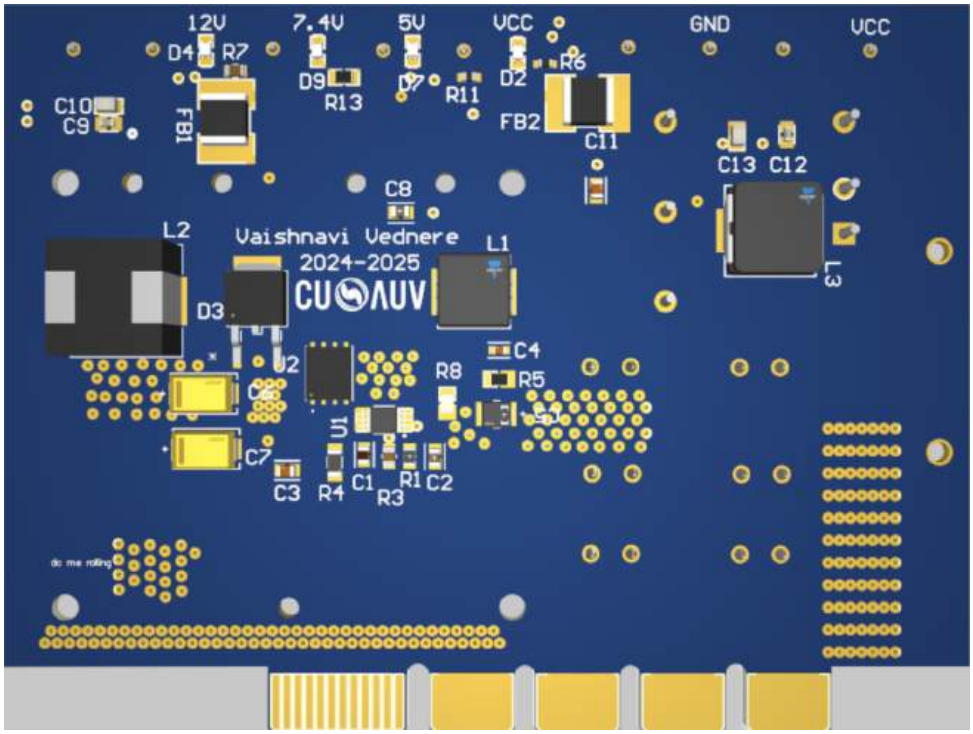
The DCDC board features three DCDC converters, two of which are trans- formers which convert 16 volts into 12V and 5V. It also consists of a buck converter to create 7.4V. There were no standard 7.4V converters. In the future, if one is interested in power electronics, they may also design the 12V and 5V channels themselves. It then outputs these voltages out of the PCIE connector. There are fuses on the board prevent overcurrent draw from any of the three channels.

Hardware

5.1 12V Channel: The CHB75-12S12 is a DCDC transformer that supplies the isolated 12 volt signal. As it uses transformer action to create the power supply, it also creates a new isolated ground. This is shared with the isolated 5 volt signal's output. This transformer has been used in previous boards including Version 6.0. The datasheet specifies values for the DCDC converter, note that the value for the inductor on v.7.0 is listed as 1.66uH, however upon looking at the actual inductor and the data sheet, this is not the right value. 1.5uH was chosen based off of the data sheet, however, I have simulated the band-pass filter and a 0.8uH inductor has better suppression of noise (attenuated at a wider-band). A lower inductor value would also be better taking into account the switching frequency of the DCDC converter (300k/400kHz). This change should be implemented and tested on the next board iteration.

5.2 5V Channel: The PDQ30-Q24-S5-D is a DCDC transformer that supplies the isolated 5 volt signal. It also creates an isolated ground that is shared with the 12 volt signal mentioned above. The values chosen in DCDC Version 6.0 were chosen to ensure similar behavior, though the datasheet was checked to ensure proper values.

5.3 7.4 Channel: The LM5085 is a DC buck converter chip that uses a switching PFET to output 7.4V. Values and components were chosen based on datasheet rec- ommendation as well as the assistance of the TI WeBench Power Designer (as recommended by the datasheet) as shown below. Values were chosen based on the design requirements of converting 16-14 volts from the battery to 7.4 volts at 6 amps. The WeBench design used as reference can be accessed using the link in A.2. The following guidelines are found in the datasheet, which should be followed: The layout must be as neat and compact as possible with all the components as close as possible to their associated pins. Two major current loops conduct currents which switch very fast, requiring the loops to be as small as possible to minimize conducted and radiated EMI. The first loop is that formed by CIN,Q1, L1, COUT, and back to CIN. The second loop is that formed by D1, L1, COUT, and back to D1. The connection from the anode of D1 to the ground end of CIN must be short and direct. CIN must be as close as possible to the VIN and GND pins, and CVCC must be as close as possible to the VIN and VCC pins.



DCDC Board.

MERGE

Abstract

The merge board manages power distribution from the two battery pods to the submarine's electrical systems. It interfaces with the battery pods through the backplane and selects the appropriate pod to draw power from based on their voltage levels. The board features two power outputs: MECHEOUT for the submarine's mechanical systems and ECEOUT for its electrical components. Additionally, the merge board incorporates a kill switch that allows power to MECHEOUT to be turned off as needed.

Design Requirements

- Board Size: 3.278 in $\times$ 4.331 in, 0.617 in from rail to connector
- Backplane Signals Used: ECE OUT, MECHE OUT, RX OUT, TX OUT
- Power: POD A, POD B, Isolated GND, Unisolated GND
- Merge two battery powers with hotswap mechanism, letting both drain in parallel
- Able to be physically killed with kill switch
- Reports current and voltage to Jetson
- Output data: RS232 UART

Design Updates

This year's merge board closely resembles last year's design, as last year's Merge was the most successful in recent history. The changes made were minor, aiming to build on that success. Firstly, the NMOS and PMOS models were updated to address soldering challenges with the small legs of the previous components. The new MOSFETs use D2PAK packages, which feature longer legs and a large drain area for easier handling. Additionally, instead of using a MOSFET to control the gate of the output PMOS, op-amp comparators are now employed. This approach reduces board space requirements and lowers impedance

High Level Description

Power originates from the battery pods, POD A and POD B. The LTC2990 voltage sensor chip monitors the voltage of each pod and sends the data to the microcontroller. From there, power enters the hot-swap mechanism, which selects the battery pod with the higher voltage at the time. The selected battery is indicated by LEDs on the board, controlled via the TLC3702 chip. Next, the current flows through a current sensor, which transmits its readings to the microcontroller. The power then moves into the channel isolation mechanism, which includes three PMOSs (two for MECHEOUT and one for ECEOUT). These PMOSs control the flow of power to MECHEOUT, ECEOUT, or both outputs. The gate of the MECHEOUT PMOS is managed by the MC74HC1G32 OR gate, which compares a kill signal from the external kill switch and the microcontroller. The kill output status is also displayed through LEDs on the board.

Implementation

The majority of the board including the MCU relies on GNDPWR, as the merge board is located before the DCDC in the power path of the sub. GND is used exclusively for the level shifter. Power enters via POD A and POD B and immediately enters hot-swap, with power for hot-swap provided directly from the batteries. Current proceeds through the current sensor and to the buck converter, which converts the approximately 16v from the batteries to 3.3v for various components on the board, including the level shifter, the OR gate, and the MCU. Data from the two onboard sensors (current and voltage) aretransmitted to the microcontroller over I2C, which then sends the signals to the Jetson via the level shifter over RS232.

Hotswap: The hot-swap mechanism is largely unchanged from previous boards. The LTC4357 work together selectively draws power from the two battery pods by controlling GATE A and GATE B of the NMOS switches. An op amp comparator activates the LED of whichever gate is currently on.

Voltage Sensor: The LTC2990 voltage sensing chip measures the voltage of the two battery pods. This offloads some computational work from the MCU by using a dedicated ADC chip. Since the voltage measurement is limited to 3.3V, the battery voltages, which can reach 16.8V when fully charged, are stepped down using a 1:7 voltage divider. The chip is powered by a +3.3V supply and communicates with the MCU via the I2C protocol using the SDA VOLTAGE and SCL VOLTAGE data lines.

Current Sensor: The ACS37800 current sensing chip uses the Hall effect to measure current. As current passes through the chip, it generates a magnetic field, which is detected and converted into a current measurement, eliminating the need for a shunt resistor. The chip supports both AC and DC applications, which is why it features VINP and VINN inputs. For DC operation, the input values are configured as specified in the datasheet. In addition to measuring current, the ACS37800 also monitors the voltage of the active battery. It operates on a +3.3V power supply and communicates with the MCU via the I2C protocol using the SDA CURRENT and SCL CURRENT data lines.

MOSFETs: The SPB80P06P PMOS and STP75NF75 NMOS are this year's merge board power switches. Their D2PAK package types will benefit us during population compared to last year. The four NMOSs (two for each battery pod) are driven by the LTC4357 chips for hotswap, and the three PMOSs (two for MECHEOUT and one for ECEOUT) are driven by KILL LOGIC for MECHEOUT and by RESTART (a microcontroller output) for ECEOUT. This year the output PMOSs use a comparator to drive their gates.

Kill Logic: The MC74HC1G32 OR gate manages the kill logic for the system. When the KILL LOGIC signal is high, the sub is in an "unkilled" state. The kill signal is provided by the external kill switch, which steps down its voltage from 7.4V to approximately 3V. Flipping the switch sets the KILL signal low, causing KILL LOGIC to go low and cutting power to MECHEOUT. If the sub needs to be restored to an "unkilled" state while physically killed, the microcontroller sets the OVERRIDEKILL signal high, which turns KILL LOGIC high and re-enables power to MECHEOUT. The current state

of the system is indicated by status LEDs. Ensure the voltage reaching the OR gate is close to 3.3V (with 3V being the expected value); otherwise, the kill switch may not function properly.

Buck Converter: The ADP2300AUJZ buck converter is powered by Vin from the current sensor (indirectly from hot-swap). It creates a +3.3V signal to be used by various circuit components.

Microcontroller: The ATXMEGA31A4U-A- microcontroller is powered by +3.3V, and has surrounding circuitry determined by the datasheet. It's clock speed is determined by crystal oscillator and refreshes at 16MHz. All data from the merge board gets transmitted to the main computer via the level shifter.

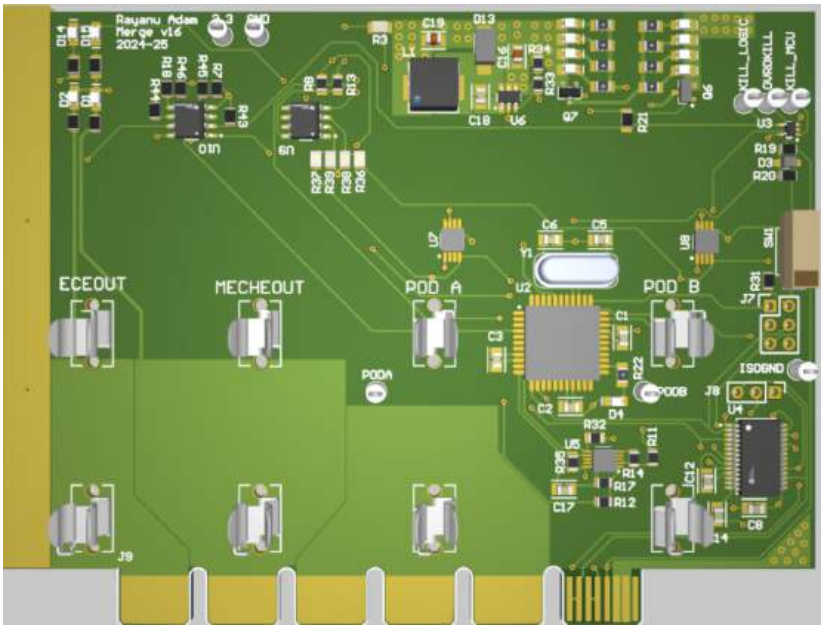
Level Shifter: The MAX3250 level shifter converts data between the microcontroller and the main computer. It is powered by +3.3V and has surrounding circuitry as determined by the datasheet. It steps up data going from the microcontroller to the main computer and steps down data coming from the main computer to the microcontroller.

Layout

Layout is the most difficult and important part of the Merge board. The board is specifically designed to minimize heat generation in both the ICs and the PCB itself. Since PCBs are not ideal for handling high power throughput, it is critical to make careful design choices when laying out the Merge board. To address this, all load-bearing traces are designed to be as wide and short as possible, as long, narrow traces tend to overheat. There are large copper pours for power. This year the larger FETs will allow for more throughput through their drains.

Software

The majority of the code adheres to standard AUV practices (such as heartbeat and TOML variable definitions, etc.). Onboard communication is handled by the AUV TWI library. The two ICs using I2C (voltage and current sensors) are connected to PORTC and PORTE, respectively. The TWI library is initialized at a 100,000 baud rate, with initialization occurring twice—once for each port. The ports are read in the checkI2CStatus method, and the values are then returned via serial communication.



Merge Board.

BACKPLANE

Abstract

I am designing this year's backplane for Orion. Backplane is the main "motherboard" that each of the team's electrical boards plugs into. It receives power from the two battery pods and provides power to the rest of the sub via the Merge, DCDC, and PD boards. It also shuffles signals to/from the Serial board via TX and RX using the RS232 protocol. Ultimately, the backplane can be thought of as the interface between the electrical system and the rest of the board.

Sample rendered view of Sirius backplane.

Design Requirements

The majority of the design considerations are the same as Sirius's backplane. I will first provide an overview of the design requirements, then go into the details of what I have changed.

Overview

Power: The system must handle the high power components of the sub. There are a variety of tools that we have historically used to minimize the load on the backplane, such as routing power directly from the ESCs to the thrusters, but there is still substantial draw when it comes to powering our systems. As such, the zones between the battery pod connectors and the merge board (which is the first board that recieves this power) must be sizable. Additionally, we use 2oz front, power, gnd, and back copper layers to minimize heat buildup. Starting last year, we implemented an air flow system designed to move heat away from the system. This system pushs air past the high power boards, which are located next to each other (MERGE, DCDC, THRUSTER1, and THRUSTER2) near the back of the sub. This system worked well, and will be maintained in this iteration. Finally, I have located boards to minimize heat buildup due to long traces. All high power components are located as close to each other as possible. I also improved the power system on Orion but addding high current connectors to the power path between the battery pods and the backplane, rather than soldering positive and negative directly onto the backplane. I will describe this change further in the hardware section.

Signal: The serial board handles all electrical system components. It is located near to the Jetson (near the front or Orion). In order to minimize potentially unreliable wiring inside of the UHPV, and as a result of the high resistance of the RS-232 protocol to noise, communication between the Serial board and the rest of the electrical system is handled by the backplane. Thus, the backplane routes TX and RX lines between the serial board and each of the other sub components that communicate via Serial. Some of these are other electrical microcontrollers, but others are external sub components. The complete list of Serial device connected via backplane are (PODA, PODB, THRUST1, THRUST2, MERGE, ACTUATORS, PD, INFRASTRUCTURE, DVL, GX, H2O, TRANSMIT, SENSOR, EXTRA 0, EXTRA 1, EXTRA 2). An additional change this year is 1 extra device -¿ 3 extra devices, maximizing the usage of the channels already present on the Serial board. External signals, like H2O, Transmit, PODA, and PODB communicate via Molex MicroClasp connectors in the connectors region of the board. There are a variety of other signals that pass through the backplane, including the kill signal, actuator pwm signals, leak sensors and more. The leak sensors will be described further in the hardware section.

Debugging / Safety Systems: Debugging on backplane primarily consistutes status leds for each of the power nets. This is largely unchanged from last year, with status LEDs located conveniently near the connectors. This year, I am adding status LEDs for PODA power and PODB power, allowing CUAUV team members to easily determine if the sub is receiving power from the battery pods.

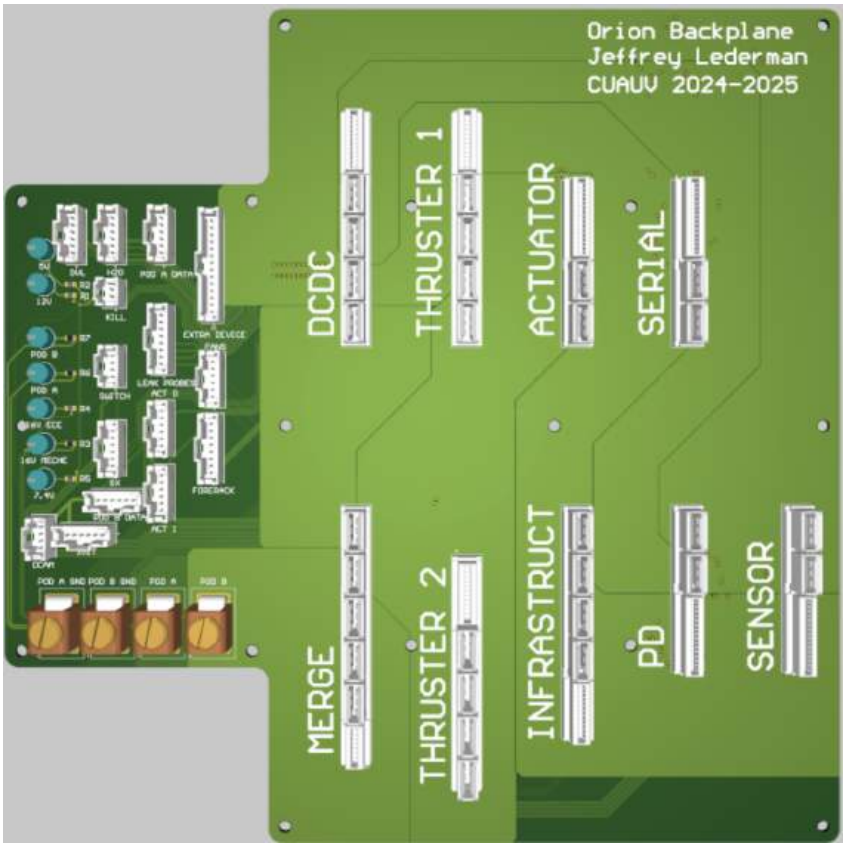
Hardware

One or the shortcomings of past documentations for backplane was a lack of a thorough accounting of the components located on the board. This is located here, and should serve as a reference for future designs of backplane.

Additional Connectors: The other key function of the backplane is to interface with the rest of the sub. It does this via the seacon panels located on the part and starboard sides of the sub. Many of the connectors located on these panels go directly to the backplane, minimizing the quantity of wires in the UHPV (with the exception of thrusters and depth, as mentioned above). The backplane connectors are all conveniently located near to the seacon panels to minimize calbe runs. These connectors are Molex MicroClasp. The following MicroClasp connectors and their uses are documented below. All connectors are of the 55932 series.:

As mentioned above, a new type of connector is used to bring power to the backplane from the battery pods. It connectors via 1932588 Phoenix Contact connectors. These are smd connectors rated for 125 amps and connect using a screw down. This eliminates the need to solder battery cables directly onto the backplane, removing a potential point of failure. This connector is depicted below:

Leak sensors: The leak sensing system is built around the Blue Robotics leak sensors, with the functionality implemented on the Sensor board. The Blue Robotics SKU for the sensors is: BR-101072. These are sponge based sensors that are pulled low if a leak is detected, relaying the signal to the merge board.



Backplane Board.

TRANSMIT

Abstract

The Transmit system serves as a transducer driver enabling inter-vehicle communication using acoustic signals. It receives data from the vehicle's main computer and converts it into an acoustic wave for the other vehicle to interpret. Building on the success of last year's prototype, this iteration is designed as a more permanent solution. However, alternative designs to further simplify Transmit's functionality are being explored for future versions.

Design Requirements

The transmit board is designed to:

- Receive isolated 12V power
- Accept raw bytes from the main computer to produce an FSK signal, with symbols represented by square waves ranging from 46 to 56 kHz
- Step up the input voltage to approximately 120V to drive the transducer
- Communicate with the main computer via RS-232
- Fit within a circular board with a 33-millimeter radius

Previous Designs

This board represents a more permanent version of last year's transmit board, incorporating hardware footprints for the experimental components added during the testing and population phase. Aside from these additions, the board retains the same logic and circuitry to operate the transducers at approximately the same frequency.

High Level Overview

The transmit board is initially powered by the power distribution (PD) board. In the previous design, the board received power via one of the spare channels on the PD board, specifically channel X1. However, the current iteration plans to dedicate a specific channel on the PD board exclusively for the transmit function. Once powered, the transmit board generates an acoustic signal when its serial write value is activated.

The board draws a dedicated 12V supply through its connector. From there, it uses two independent low dropout regulators (LDOs) to produce stable 3.3V and 12V supplies for various components. The 3.3V powers the microcontroller and the level shifter, enabling communication with the main computer, while the 12V powers the gate drivers, MOSFET channel, and transformer.

When the serial write value is enabled, the microcontroller generates two identical square waves at distinct frequencies to represent binary 0 and 1. Since these signals alone lack sufficient current to drive the MOSFET, they are routed to individual gate drivers. These gate drivers amplify the signals and control the MOSFET, which drives a high-frequency step-up transformer that powers the transducer.

The transducer consists of a piezoceramic ring embedded in a waterproof material. This ring is housed separately from the main transmit enclosure and is connected via a cable penetrator. To ensure minimal energy loss in the acoustic signal, the potting material surrounding the ring should ideally match the acoustic impedance of water. Currently, the transducer uses a urethane potting compound, which has proven to be an effective choice. Preliminary exploration of alternative materials has been limited due to high costs and long lead times, but further testing will be conducted once the board is fully operational.

Implementation

Supply Circuitry: The board employs an NCP1117 fixed LDO voltage regulator to create the 3.3V rail for the MCU and serial level shifter. Additionally, an LMP78-12-1 DC-DC converter is used to provide a stable 12V rail to drive the transducer circuitry. This converter ensures the board maintains a consistent 1-amp current, simplifying the calculations for power delivery through the transformer to drive the transducer. To prevent overcurrent, a 1.1A fuse is also integrated into the design.

Modulator and Serial Path: To generate the FSK signal, the system incorporates a modulator that alternates between frequencies to produce the desired output. This is implemented on the ATxmega32A4 microcontroller, which generates a PWM signal where the frequency represents the transmitted symbol. A higher-voltage RS-232 signal from the main computer is sent to the board, then converted to a lower 3.3V TTL signal using a MAX3240 level shifter for compatibility with the MCU. This conversion ensures the serial signal is less vulnerable to external noise while remaining easy for the microcontroller to process.

Unlike earlier models, this board utilizes two pins from the MCU for modulation instead of one. Previously, a single wave modulator signal drove both the gate driver and power transistors, increasing the risk of cross-conduction at the inverted FET. This occurred when all transistors in the FET's H-bridge configuration were on simultaneously, causing damage. To address this, a secondary wave modulator signal and gate driver were added, allowing deadtime to be incorporated into the MCU firmware. This ensures proper transistor switching and prevents cross-conduction.

Transducer Driver: The MCU's PWM output is sent to an MCP14A0052 gate driver, which provides the required voltage and current for optimal transistor switching. These gate drivers, in turn, drive AO4629 power transistors that feed the transformer. Since the transistors only function with a positive voltage, a voltage offset (DC bias) is applied to the CMOS inverter to maintain proper operation. However, this DC bias introduces a low-frequency AC current into the signal, which can accumulate within the transistor and cause the transformer to fail.

To address this, a capacitor is placed in series with the transformer, acting as a high-pass filter to eliminate low-frequency AC current. The capacitor's value is selected so the center frequency of the LC circuit, formed by the capacitor and the transformer's inductance, is well below the operating frequency. A higher capacitance is chosen to achieve this effect. The transformer also retains built-in current, which must return to the supply when the transformer is turned off. Since the FETs cannot switch quickly enough to redirect this current back into the circuit, additional Schottky diodes are added in parallel with the body diodes. These Schottky diodes have a low forward voltage and fast switching capability, allowing excess current to flow back to the 12V supply while preventing voltage spikes across the transformer.

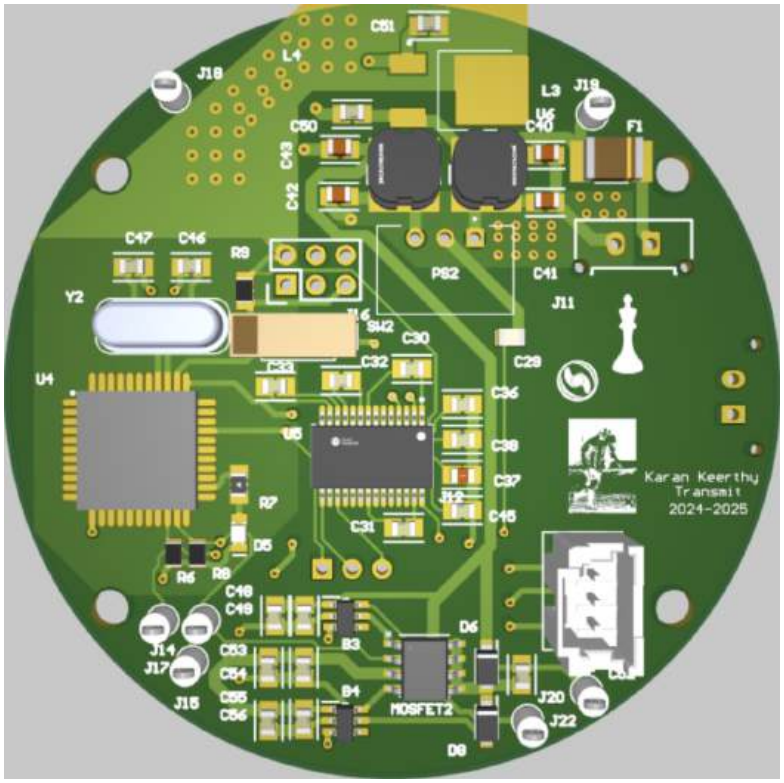
To further protect the board, additional capacitors are placed at each FET gate. These capacitors store any excess energy from the transformer, preventing other components on the board from receiving excess current and thereby enhancing their protection.

Software Walk-Through

The main sub-computer prepares a data packet containing the word to be transmitted and sets the frequency for its transmission. The code first verifies that the packet is properly formatted and that the data is correctly initialized according to the number of encoded bits per symbol. Once validated, the packet is sent through one of the microcontroller's output pins to the gate drivers, which then enable the transformer.

An interrupt service routine (ISR) regularly checks whether the current packet has been fully transmitted. Once transmission is complete, the ISR retrieves the next valid packet from a queue of waiting packets and sends it to the output. If an invalid packet is detected in the queue, it is removed and ignored. When the packet queue is empty, the output pin is disabled to prevent accidental activation of the transformer.

While managing the transmission and clearing of data packets, the microcontroller also runs the heartbeat code concurrently to ensure the board's normal functionality throughout the process.



Transmit Board.

INFRASTRUCTURE

Abstract

The Infrastructure Board is primarily used for debugging, operating 3 LED strips that can be configured to indicate characteristics of the sub. Two of the strips are found on the side of the sub's hull, while the other provides downward camera lighting. The board also controls three 30mm 5V fans for cooling. While not exactly critical to Orion's functionality, Infrastructure is able to make its operation a little bit smoother.

Design Requirements

- Receive 16V power supply and convert to appropriate levels for various components.
- Receive RS-232 signals from backplane and convert to PWM signal for LEDs
- Operate 2 NeoPixel RGB LED strips
- Operate 1 KXYM COB LED strip
- Visually indicate when correct voltages are being supplied to board components
- Include test points for debugging

Previous Designs

In the past this board was called LED as its functionality was limited to operating the strips for debugging, but after capabilities like the fans were added it was renamed as Infrastructure. Compared to last year the changes to Infrastructure are fairly minor, consisting of layout optimizations and replacing a capacitor and fuse that were causing issues.

High Level Description

Infrastructure operates at 3 voltage levels that are used to power components. 16V is provided by Merge Board through the backplane and is immediately dropped down to 5V by a DC/DC converter, which provides the power to the LEDs and fans. An LDO then converts 5V to 3.3V to supply the microcontroller. In addition to these power signals, Infrastructure also recieves RS-232 data signals through the backplane. The level shifter and microcontroller work to convert these to 3.3V PWM, which are stepped up to 5V by the isolator and used to control the LED strips.

Implementation

Backplane Connector: The backplane is how the board connects to the rest of the sub, supplying Infrastructure with 16V Vcc power, GND and ISOGND, and RS-232 signals.

Level Shifter: The MAX3250 Level Shifter converts the RS-232 signals supplied by the backplane to UART signals that can be used by the microcontroller.

Microcontroller (MCU): The ATXMEGA32A4U microcontroller generates the PWM signals that control the LEDs.

DC/DC: The I6A24014A DC/DC converter drops the Vcc voltage of 16V down to 5V to power the fans and LEDs.

Low Dropout Regulator (LDO): The LM3940 LDO takes the 5V generated by DC/DC and steps it down again to 3.3V, which is what powers the microcontroller.

LEDs: The board connects to two NeoPixel RGB strips with a density of 60 LEDs per meter. The KXYM COB strip has a density of 320 LEDs per meter and can only produce white light.

Fans: Infrastucture has 3 5V 30mm fans to provide cooling for the sub, which are controlled by the MCU through an NMOS transistor.

Layout

Infrastructure is a 4 layer board with the front and back layers used to mount components and the middle two for ground and power layers. The ground layer has two zones for GND (corresponding to power signals) and ISOGND (data signals). The ISOGND layer is considerably smaller as it really just needs to connect the serial header and level shifter to the ISOGND provided by the backplane. For the power layer, there are the 3 zones mentioned earlier for 16V, 5V and 3.3V. This board has a lot of vias, which is a good thing to make sure powerful signals have a large enough area to pass through, but what I did in the bottom left of this board is definitely overkill.

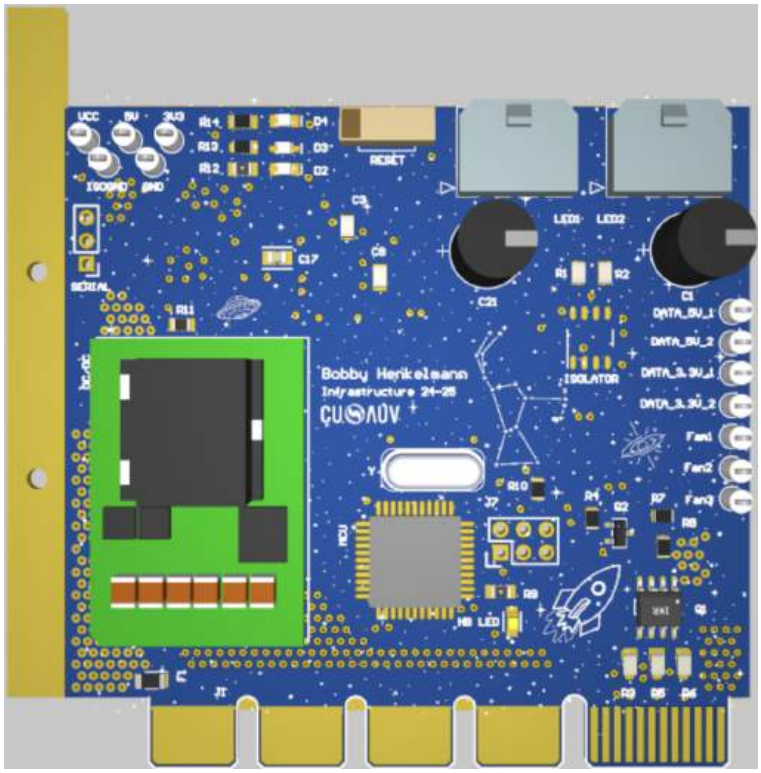
Software

Infrastructure's code is organized into a main file (led.c), a header file (led.h), and a communication file (led.toml).

Setup

The setup() method initializes the microcontroller, configuring the 16MHz crystal and designating PD4 as an output pin. LED setup is taken care of by a separate setupLED() method.

Updating LEDs An RGB struct is used to store the color information of each LED, where colors are represted by 8 bit integer values. These values can be updated by software through serial input.



Infrastructure Board.

THRUSTER

Abstract

Thruster board utilizes 4 electronic speed converters (ESCs) to control each of the submarine's underwater thrusters. The job of the board is to provide each ESC with 16V and a PWM signal to power and control the speed of the associated thruster. Two boards are used on the submarine to control a total of 8 thrusters.

Design Requirements

- Control 4 Blue Robotics T200 Brushless DC Thrusters using 4 Blue Robotics 30 A Basic ESCs
- Communicate with the 4 ESC modules via PWM from the ATXMega microcontroller
- Provide 16 V of unisolated power and unisolated ground for the ESCs and Thrusters
- Power an ATXMEGA microcontroller with a 3.3 V power line given an input voltage of 7.4V
- Communicate with the main computer of the vehicle over RS-232
- Provide test points for debugging purposes
- Need to confirm dimensions

Previous Designs

The biggest change in the Thrusters v12 is the move from a linear LDO to a buck converter for generating 3.3V. In the past, the TPS7A4533 LDO was used to step 7.4V down to 3.3V, but it burned off a lot of excess voltage as heat. Switching to a buck converter significantly reduces that power loss and helps keep the board cooler and more efficient overall.

Another practical improvement is the relocation of the reset switch. In earlier designs, the reset button was hard to reach once the board was mounted inside the vehicle, which made debugging annoying. The new placement makes it much easier to access during testing and development without needing to pull the board out. Additional layout improvements were made for better routing and accessibility.

High Level Description

The Thruster Board interacts with the rest of the submarine through the serial RX/TX lines via the backplane. The backplane also provides unisolated 7.4V and 16V power, as well as both unisolated and isolated ground connections. The 7.4V unisolated power is stepped down to 3.3V using a buck convertor in order to power the microcontroller (MCU) and level shifter. The level shifter moves the RS232 RX input from the backplane to TTL RX for the MCU. On the reverse, it turns the TTL TX from the MCU to the higher voltage RS232 to go back through the backplane. The data from serial tells the microcontroller the desired duty ratio for each thruster. Using this, the microcontroller generates pulse width modulated (PWM) signals which it sends to the ESCs. The ESCs are also provided with the 16V power line to power the thrusters.

The thrusters are controlled via a method known as Trapezoidal Control. Each thruster features three electromagnetic coils labeled A, B and C. At a given point in time, one of these coils will be high (receiving current), one coil will be low (current exits through the coil, serving as ground), and one coil will be off. The ESCs interpret the PWM signal from the microcontroller and sets coils A, B and C to high, low and off by controlling the current through each coil. A higher PWM duty cycle means faster switching between coil combinations, which increases the thruster's speed.

Implementation

Backplane Connector: The Thruster Board connects to the rest of the vehicle through a backplane connector, which supplies the board with power and communication lines. Specifically, it receives unisolated 16V power for the ESCs and thrusters, 7.4V for onboard electronics, RS-232 RX and TX lines for serial communication, and both isolated and unisolated ground planes. The power and signal lines are routed to their respective subsystems via internal copper planes and traces. GNDPWR is used for high-current components such as the ESCs, while the isolated ground is used for sensitive serial communication to minimize noise.

Buck Convertor: To provide 3.3V power to the logic components, the 7.4V line is stepped down using a ADP2300AUJZ-R7 buck converter. This switching regulator replaces the linear LDO used in previous designs, significantly improving power efficiency and thermal performance. The buck converter uses an inductor, diode, and output capacitor network to maintain a stable 3.3V output, which powers both the microcontroller and level shifter. Careful layout considerations, including ground plane separation and decoupling, are used to minimize ripple and noise.

Level Shifter: The MAX3250 level shifter handles voltage translation between the board's TTL logic and the RS-232 serial protocol. The RX and TX lines from the backplane are routed through the level shifter. It converts the incoming RS-232 RX signal to 3.3V TTL for the microcontroller and boosts the TTL TX signal from the microcontroller back up to RS-232 levels for return transmission. The level shifter is referenced to the isolated ground to prevent communication interference from high-current devices on GNDPWR. A serial header is also included for bench testing and debugging.

Microcontroller: At the core of the Thruster Board is the ATxmega32A4U microcontroller, which is powered by 3.3V and connected to the TTL-level RX and TX lines from the level shifter. It receives serial commands containing values for each thruster. The microcontroller is programmed in C and uses a timer module powered by the crystal to generate four separate PWM outputs, one for each ESC. These PWM signals control the speed of each thruster. The board includes a programming header, reset switch, and heartbeat LED for in-field programming, resets, and basic system status indication. All are placed near the board edge for easier access during integration.

ESCs: Each of the four Blue Robotics Basic 30A ESCs is responsible for controlling a single T200 thruster. ESCs receive three inputs: 16V power, GNDPWR, and a PWM control signal from the microcontroller, and output the alternating A,B and C coils. ESC outputs are routed through microfit connectors to the thrusters using external wiring. The ESCs are mounted directly to the PCB using through-hole pads with thermal reliefs to balance solderability and current-carrying capacity.

Layout

This board kept most of the layout advancements made on V11. To ensure that the ESCs could be easily soldered and de-soldered from their through-hole pads, the pads were selected for thermal relief, allowing enough copper connection to provide the necessary current, but also preventing all the heat from a soldering iron dissipating in the large GNDPWR and +16V copper planes.

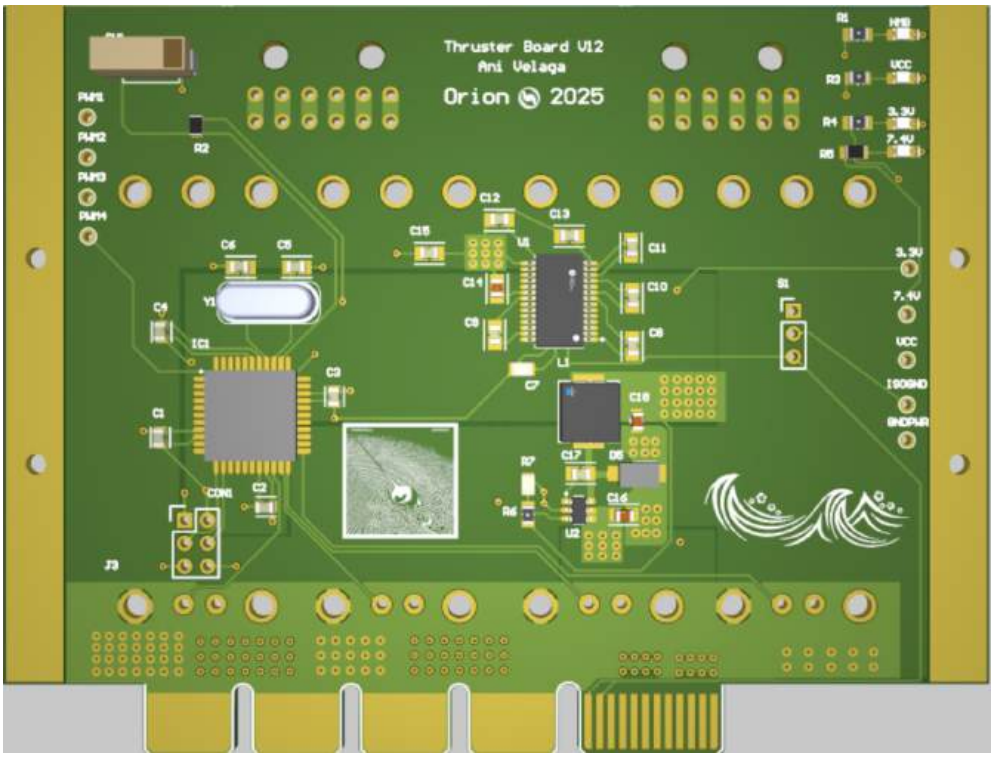
It also re-utilized the rail system which was designed to keep ESCs in the path of airflow to dissipate as much heat as possible from the high-voltage components. This board saw the reset switch being moved to the top of the board to be more easily accessible once installed in the sub.

Software

The main software in this board is the standard serial communication and heartbeat execution. Heartbeat is ran through the PDI header and indicates that the microcontroller is executing instructions properly by toggling a status LED at a fixed interval.

The Thruster Board is responsible for regulating the thrusters, maintaining the desired duty cycles specified by the main computer via serial communication. The microcontroller uses its internal Timer/Counter modules to generate four PWM signals—one for each ESC. These outputs are configured in hardware. The duty cycle of each signal is updated based on the values received over serial, allowing dynamic control of thruster speed in real time. Initially, the PWM signal starts in a high state at the beginning of each cycle.

For each ESC, four compare channels are utilized to update the PWM signal. A counter, incrementing from the BOTTOM value to the TOP value, is continuously updated every two milliseconds using a timer-triggered interrupt. Each compare channel constantly compares the counter value with the period stored in the register. If they are equal, an interrupt is generated, indicating the end of the duty cycle and causing the PWM signal to transition to a low state.



Thruster Board.

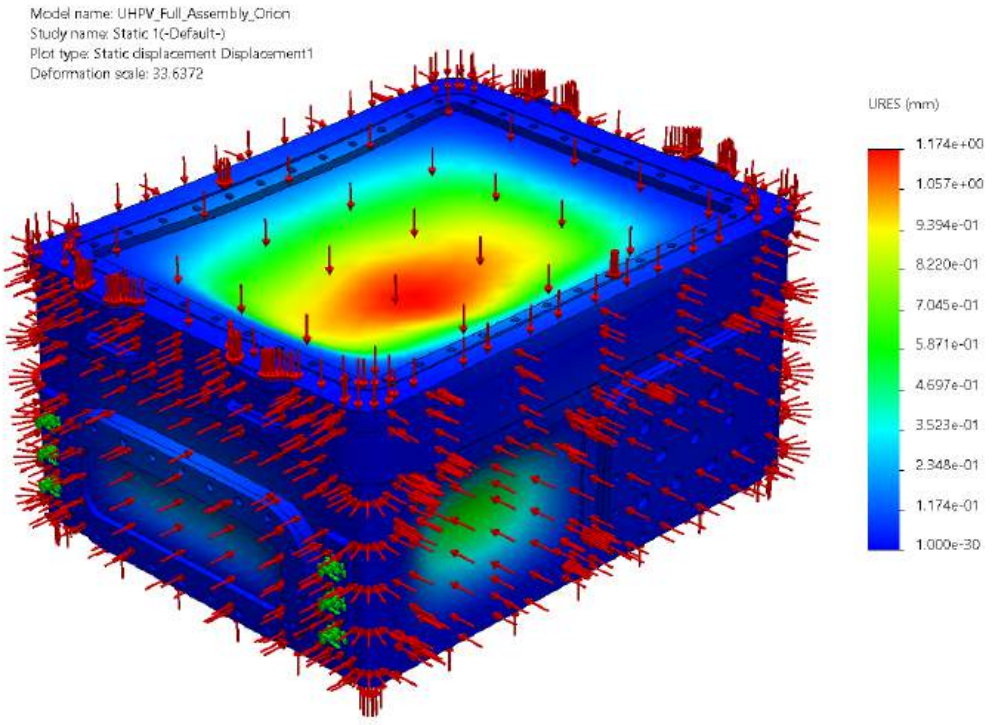
APPENDIX
C: MECHANICAL

Orion Manipulator Overview

The Orion Manipulator is a modular, quickly reconfigurable gripper designed for the CUAUV's Spring 2025 competitive mission. Building on the Fall 2024 manipulator library, it introduces an adaptable capture module optimized for irregular, cylindrical objects. Its three-part construction—bottom housing with dowels, gears, and master screws; middle plate with mortise-fit gear hoops; and top assembly for servo and pressure transducer mounting—allows rapid disassembly and reassembly. Special attention is given to dowel placement, quick-release pin alignment, and filament choices to ensure precise, repeatable operation.

Integration, Operation, and Testing

Installed adjacent to the DVL, the manipulator requires careful cable routing to avoid sensor damage. Operators must verify that the servo gear meshes cleanly with both hoop-gear assemblies before energizing to prevent gear failure. Field adjustments—such as re-drilling quick-release pin holes for new filament prints—ensure ongoing precision. Water-bucket trials confirmed reliable pick-and-place performance on standard objects (e.g., cups), with TPU elastic extensions enabling delicate grips; spoon retrieval demands a controlled approach to engage the capture rods. Stability and holding torque proved sufficient. A detailed parts list (heat-set inserts, nuts, screws, dowels, quick-release pins, and recommended PPA-CF filament) is provided to support fabrication and maintenance.



Deformation Simulation.

In addition to the 15 psi structural FEA (16,440 psi max stress, 2.43 FOS, 0.046 deformation), the UHPV underwent complementary analyses to de-risk integration. Modal analysis showed the first natural frequency above 180 Hz, well clear of thruster excitation bands, minimizing vibration-induced o-ring

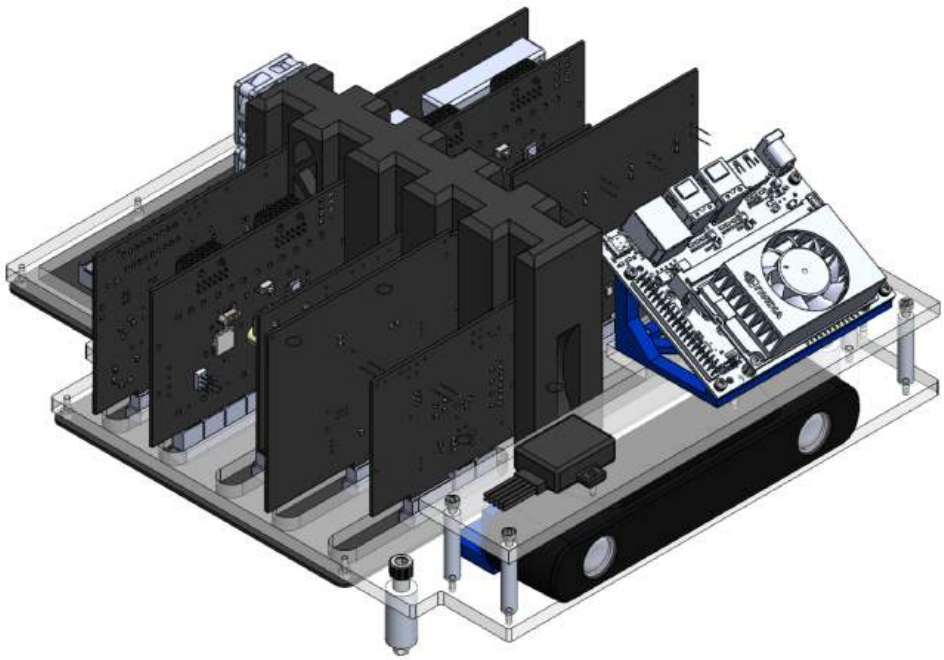
fatigue. Thermal FEA—assuming 15 W internal dissipation from the Jetson and boards—predicted a peak hull temperature rise of 8 °C over ambient, confirming that passive conduction through the aluminum hull maintained all components within safe operating limits. O-ring groove chamfer angles were iterated in simulation to optimize ease of lid engagement without compromising seal compression.

Orion UHPV Overview

The Orion Upper Hull Pressure Vessel (UHPV) is a lightweight, rectangular "lunchbox"-style enclosure designed to house the Jetson, circuit boards, forward-facing ZED camera, depth sensor, and killswitch while providing reliable watertight seals via bore and face o-ring grooves. Building on Sirius's lessons, Orion minimizes weight by slimming the hull dimensions (11.7" × 15.55" × 6.95"), swapping to larger-cross-section 300-series o-rings with optimized groove chamfers, and replacing welded panels with fully subtractively-machined CNC parts (lid in-house, flange and SEACON bulkhead panels via Datron, hull via Xometry with CMM inspection). SEACON connectors are arranged in compact 3-3-4 arrays on port/starboard panels, and the killswitch panel now uses a Binder 770 tether bulkhead and BlueRobotics Bar02 depth sensor for simplified, reliable integration. Split handles, acrylic viewing windows, and detailed o-ring analysis (Appendix C) further enhance serviceability and seal performance.

Manufacturing, Status, and Path Forward

Orion's production plan balances in-house control over critical tolerances (lid machining and acrylic laser-cutting) with outsourced efficiency for large, complex parts. Following winter-break fabrication, assembly and leak testing will commence early spring, guided by a tighter project timeline and insights from Sirius's delays. Finite element analysis at 15 PSI predicts stress (16,440 PSI), safety factor (2.43), and deformation (0.046") on par with successful predecessors. Looking ahead, recommended process improvements include earlier UHPV design kickoff (pre–fall semester), selective exploration of soft-durometer or alternative-cross-section o-rings, and year-by-year evaluation of rectangular vs. cylindrical formats based on buoyancy, balance, and machining resources. This cautious, iterative approach aims to deliver a robust, serviceable pressure vessel ready for rapid integration and competition testing.



Orion Racks CAD.

Orion Racks Overview

The Orion racks subsystem delivers a compact, serviceable mounting solution for all electronic hardware housed within the Fall 2025 Orion UHPV—custom PCBs, Jetson computer, ZED camera, depth sensor, and switches—while also supporting standalone bench testing. Building on Polaris's dual fore/aft cylindrical racks and Sirius's rib-cage backplane design, it meets tight UHPV constraints by prioritizing minimal weight, reduced machining, vibration control, thermal clearance, and optimized trace routing. The core requirements—fit within Orion's smaller rectangular UHPV, secure frame attachment, easy component access, and out-of-sub functionality—guided every layout and material choice.

Design Details, Status, and Next Steps

The assembly breaks into four modules: a laser-cut acrylic backplane support shortened by trimming non-cooled board spacing; an FDM-printed "Cooling Tower" with wedgelocks and a curved top for cable routing; a front mounting acrylic panel repositioned above the ZED camera (now overhung) with the Jetson at a steeper angle; and an MDF "Test Bench" board with tapped holes for out-of-sub troubleshooting. Static (1,954 psi max stress, 6.14 safety factor, 0.0116" deflection) and vibrational FEA validate the backplate's integrity. Full fabrication is scheduled for January's machine shop campaign, with electrical integration by mid-February. The design's absence of bespoke machine parts ensures rapid iteration, and its modular, acrylic-centric approach will serve as a reference for future CUAUV rack developments.